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Project 3

RETRODIRECTIVE TRANSPONDER FEASIBILITY EXPERIMENT

October 1967

Prepared under

Contract No. NAS 8-21078

Engineering Studies and Analyses on Systems, Subsystems and Related Interface Optimization Problems

for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

This document constitutes a Final Technical Report for Project 3, "Retrodirective Transponder Feasibility Experiment," prepared under Contract #NAS8-21078 entitled "Engineering Studies and Analyses on Systems, Subsystems and Related Interface Optimization Problems." The purpose of the experiment described in this report is to test and verify the practical feasibility of the digital phase measuring subsystem of the pulse-coherent retrodirective transponder. A general discussion of retrodirective antenna arrays and pulse-coherent transponders, and a description of the digital phasemeter portion of the pulse-coherent retrodirective transponder have been given in earlier ADCOM, Inc. Technical Memoranda.[1,2] The second of these documents[2] showed that the essential features of the overall transponder operation could be effectively demonstrated by implementation in a laboratory test set-up of the IF and digital phasemeter portion of the proposed transponder design. This basic approach is justified by the straightforward design characteristics of the remaining portions of the transponder circuitry. Some of the other portions include standard microwave circuits, frequency converters and microwave power stages.

This present document includes:

(1) Technical background comprising a review of the overall transponder operation and of the digital phasemeter operation.

(2) Description of the phasemeter test bed including block diagrams and brief equipment descriptions and a discussion of the phasemeter timing sequence,

(3) A description of the experimental procedure,

(4) Experimental results showing the transponder output phase error as a function of input SNR, and

(5) Conclusions and recommendations derived from the experiment.

2. TECHNICAL BACKGROUND

When microwave antennas are deployed on a spacecraft whose characteristic dimensions are large compared with the operating wavelength, problems arise as to the most desirable configuration in which to employ the antennas and their associated transponders. The antennas can be operated coherently, i.e., excited by a common microwave power source. They can be excited separately, each by its own transponder, or they can be operated one at a time under the control of some decision circuitry. Each of these regimes has associated problem areas. Coherent excitation gives rise to an interferometer-like pattern structure with deep radiation pattern minima which can cause signal loss for substantial periods even with transponder augmentation. Incoherent operation increases on-board weight and power drain, and interference between pulses from separate antennas can cause substantial range errors even at short ranges. Both these approaches additionally waste power by uncontrolled radiation into portions of space inaccessible to the interrogator. Single element excitation under control of decision circuitry prevents possible gain enhancement by coherent antenna combination, but is otherwise the best of the approaches listed here, although the improvement is obtained at the expense of increased on-board complexity.

The present design effort employs a retrodirective array technique which has several advantages. First, maximum possible gain (within the quantization error) is obtained in the direction of the interrogator; second, radiation into undesired portions of space is precluded; and third, increase in on-board equipment is moderate. It should be noted that the increase in on-board equipment can be traded off against reductions in on-board power requirements made possible by the first two design features. Finally, the design is compatible with pulse-coherent doppler tracking requirements.

2.1 The Pulse-Coherent Retrodirective Array

The operation of the pulse coherent transponder is based on the method of conjugate phase. Phase conjugacy is a condition for retrodirectivity as can be shown by reference to Fig. 1.

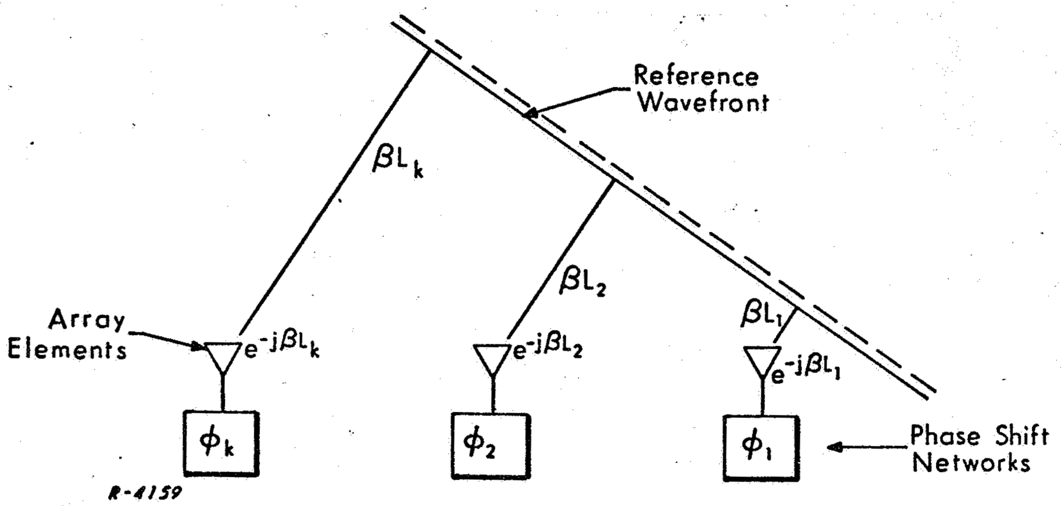


Fig. 1 Array Phase Relations

The phase at the input to the kth element relative to the phase angle at the reference wavefront is βL_k, i.e., the propagation factor for the incoming wave at the kth element is $e^{-j\beta L_k}$. After passing through a network which adds a phase shift ϕ_k, the phase angle at the output of the kth element is $(\beta L_k + \phi_k)$. After propagation to the reference wavefront, the phase angle becomes $(2\beta L_k + \phi_k)$. In order for the reradiated phase front to coincide with the incident phase front the phase of each reradiated signal must be a constant which may be taken as 0^o. Therefore

$$\begin{aligned}(2\beta L_1 + \phi_1) &= (2\beta L_2 + \phi_2) = \ldots \\ &= (2\beta L_k + \phi_k) \\ &= 0.\end{aligned}$$

Solving for ϕ_k and substituting into the expression for the output phase of the k^{th} element gives $e^{j\beta L_k}$, the complex conjugate of the input signal.

This principle is implemented in the pulse-coherent retrodirective array. The antenna elements can be mounted on a surface of arbitrary curvature and the design is particularly suited for random-access operation at a very high repetition rate which can be expected when multiple ground interrogators are used. A block diagram of the transponder is shown in Fig.2. In this figure the transmitting and receiving elements are shown separately for clarity although in practice transmit and receive modes would share common antennas. The operation is as follows: Element 1R feeds a pulse-coherent transponder which is of a standard operational design. The output of the TWT of this transponder, after phase shifting at each of the other modules, will be retransmitted from all other elements. The signal received at element 2R is the same as that received at element 1R except for a time delay (phase shift) which is a function of the incoming wave arrival angle. Since both signals are mixed with the same L.O. and both are amplified in similar IF amplifiers, the phase difference between the two can be detected in a phase detector as shown in Fig.2. Similarly the phase difference between the 1R and 3R signals can be detected, etc. The digital phase detectors used for this purpose are the same as those used in octonary PSK communications receivers. The binary word output is operated on so that the corresponding phase is reduced by 180°, i.e., conjugated. This can be performed in a simple logic circuit or the operation can be performed implicitly by the digital phase shifter which interprets the binary word. The time required to measure the phases of the received signal and to set the digital phase shifters to the proper values is available because the TWT output is delayed by δ sec. δ is usually chosen to be around 5 to 10 μs. When the pulse appears at the output of the

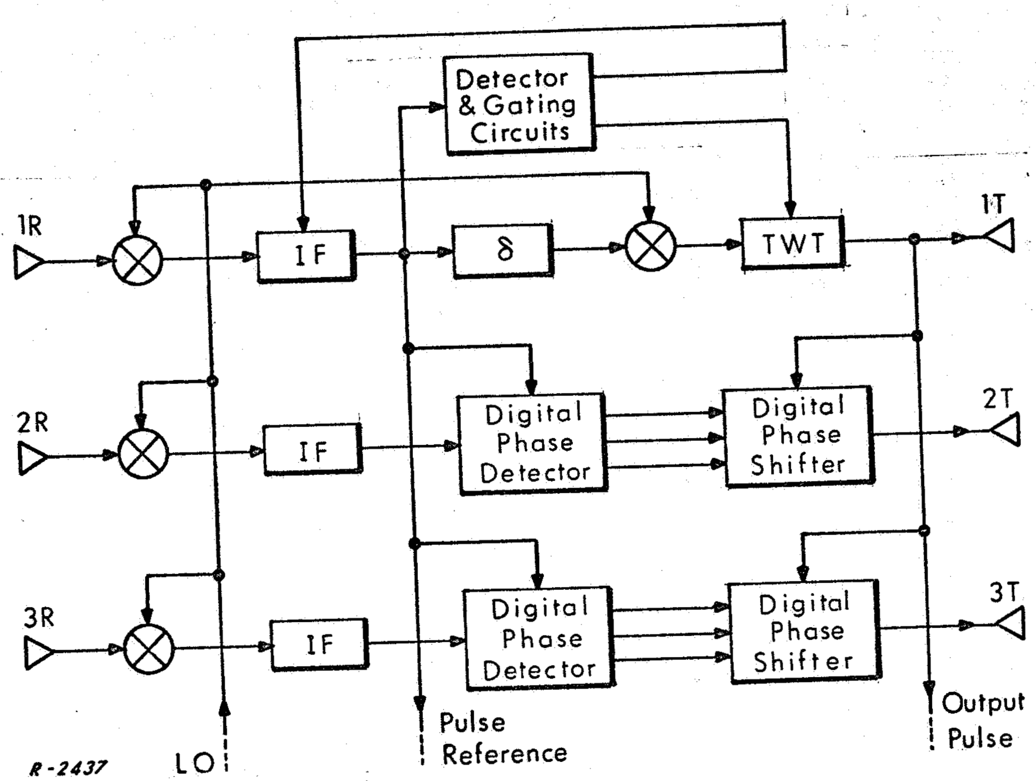


Fig. 2 Pulse-Coherent Retrodirective Transponder

TWT, it is distributed to each of the preset digital phase shifters which assure that the phases of the pulses at each of the transmitting elements are correct for retrodirectivity.

An important consideration in the operation of devices of this type aboard space vehicles is the minimization of power drain. System keying must be incorporated in any practical design and Fig. 2 also illustrates the system keying principles.

In the absence of an input pulse the gating circuitry (gate generators, pulse modulators, etc.) is not triggered. Under this condition the IF preamplifier is operative while the TWT chain is fully cut off. When a pulse of adequate signal strength is received, a pre-trigger is generated in approximate time synchronism with the pulse leading edge. The pulse is also applied to the IF delay line. While this pulse is in storage in the delay line, the gating circuitry disables the IF preamplifier. Also, during this period the digital phase meter measures the relative phase in each antenna line and sets the corresponding digital phase shifter. Just before the stored pulse emerges, an ON trigger is generated, turning on the TWT chain for a sufficient time to allow for pulse transmission. After transmission the original conditions of minimum power drain are restored. Using this keying technique the possibility of ring-around is minimized, since the complete transmit-receive loop is never closed at the same time.

2.2 Operation of Digital Phase Meter

The digital phase meter is shown in Fig. 3.[3] As has been noted previously, the digital phase meter is the critical element in the proposed retrodirective pulse-coherent transponder. The function of the digital phase

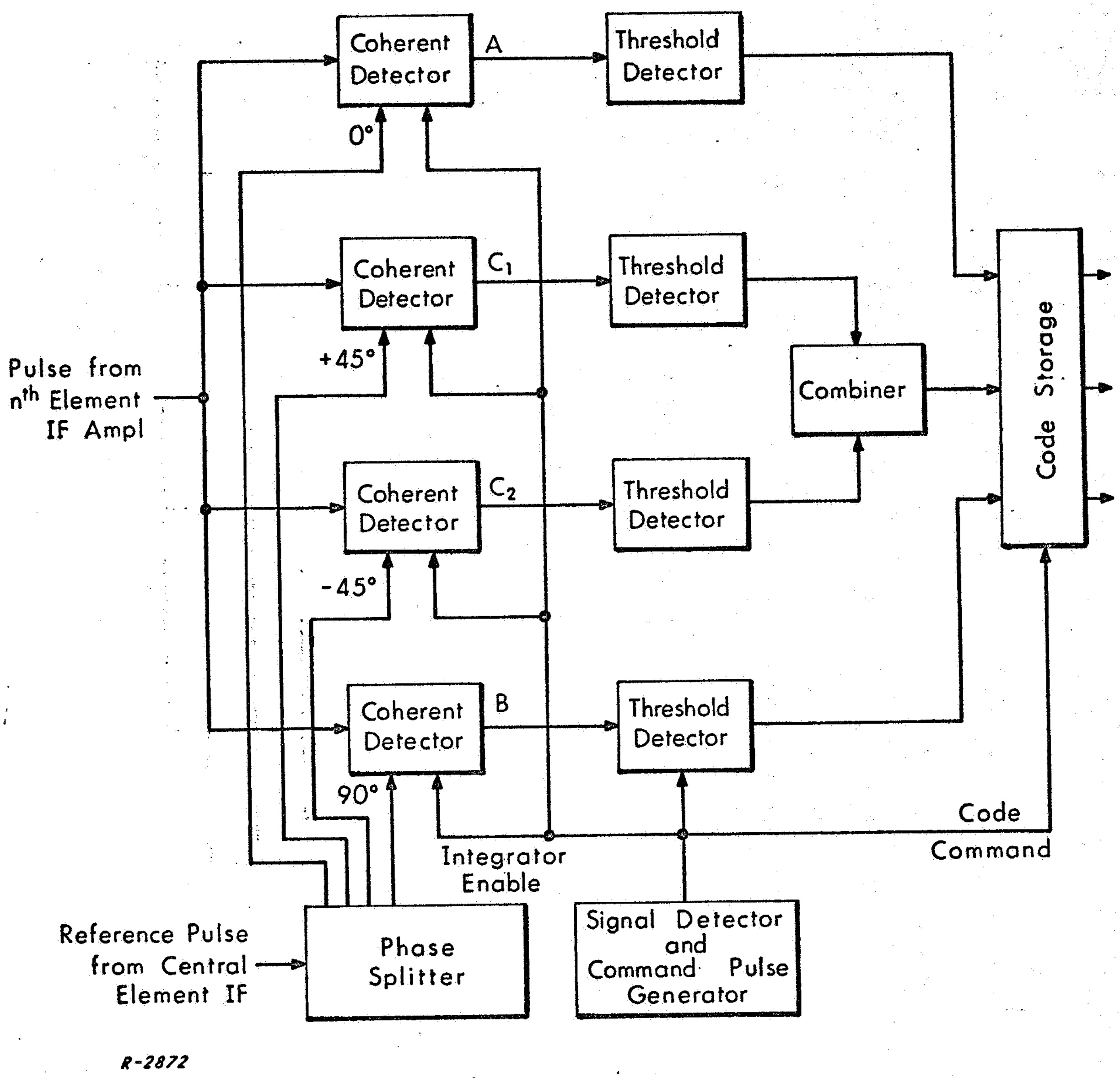


Fig. 3 Digital Phase Meter

meter is to measure the phase of the received signal at each antenna relative to the phase at a designated reference antenna. This relative phase can be determined using a device which has found application in digital PSK systems, that is, the octonary detector. An octonary detector is suitable for this application because its output is quantized in 45^o increments. Thus, the quantization error is at most $22\text{-}1/2^o$, and this error does not have a serious effect on the gain of the array on retransmission.

The operation of the digital phase meter is now described with reference to Fig.3. The reference pulse is passed through a phase splitter to produce four pulsed signals with relative phases; 0^o, $+45^o$, -45^o and 90^o. The received pulse at the n^{th} element is fed to four coherent detectors. The outputs of the detectors are sampled at a time determined by a signal arrival detector. This is a device which monitors and averages the outputs of envelope detectors in each of the elements IF amplifiers. At the sampling time, the polarity of the voltage at each of the four coherent detectors is determined. For example, if the voltage at A in the figure is positive, the relative phase is between -90^o and $+90^o$. Similarly, if it is negative, the relative phase is between $+90^o$ and 270^o. The output at B is used to determine if the phase is between 0^o and 180^o or between 180^o and 360^o. Thus, combining the results of these measurements determines the quadrant in which the relative phase lies. Examination of the outputs at C_1 and C_2 determines which half of the appropriate quadrant contains the phase. If A and B are both positive, the phase is between 0^o and 90^o. Then, if C_1 and C_2 are both positive, the phase must be between 0^o and 45^o. If C_1 is positive and C_2 negative, the phase must lie between 45^o and 90^o. A complete tabulation of detector outputs, phases and binary coded outputs is shown in Table 1.

Table 1

PHASE DETECTOR OUTPUTS

Phase	A Output	B Output	C_1 Output	C_2 Output	Binary Number Output
$0^\circ - 45^\circ$	+	+	+	+	111
$45^\circ - 90^\circ$	+	+	+	-	110
$90^\circ - 135^\circ$	-	+	+	-	010
$135^\circ - 180^\circ$	-	+	-	-	011
$180^\circ - 225^\circ$	-	-	-	-	001
$225^\circ - 270^\circ$	-	-	-	+	000
$270^\circ - 315^\circ$	+	-	-	+	100
$315^\circ - 360^\circ$	+	-	+	+	101

3. DESCRIPTION OF DIGITAL PHASE METER TEST BED

This section describes the experimental arrangements for testing the digital phase meter. The section is divided into two parts; the first discusses the overall experimental arrangements and describes the function of each block of the overall system block diagram including peripheral experimental equipment and measuring apparatus; the second part is devoted to an exposition of the timing sequence of all events involved in making a digital phase measurement on a single incoming pulse.

3.1 Experimental Set Up and Test Procedure

Figure 4 illustrates the experimental test bed incorporating the digital phase meter, pulse generating and phase shifting circuitry, IF circuitry, gray to natural code converter, D/A converter, and provision for addition of noise in the reference and signal channels independently. As has been noted earlier, it is sufficient to verify only the IF pulse detection portions of the circuitry since the microwave portions are straightforward and are in general operational use. An IF frequency of 30 MHz was chosen since standard commercial components are readily available at reasonable cost for this frequency. The simulated input signals are produced at 30 MHz in the following way. The signal source is a commercial 30 MHz signal generator whose output is divided and applied to a pair of balanced modulators M_1 and M_2. The upper path in the figure providing the input to modulator M_1, as shown, first passes through the switched delay line sections to provide relative phase shift between the reference and signal channels. This phase shifter is implemented by switched interconnections between fixed coaxial sections. These interconnections allow for the introduction of phase shifts in every quadrant between 0^o

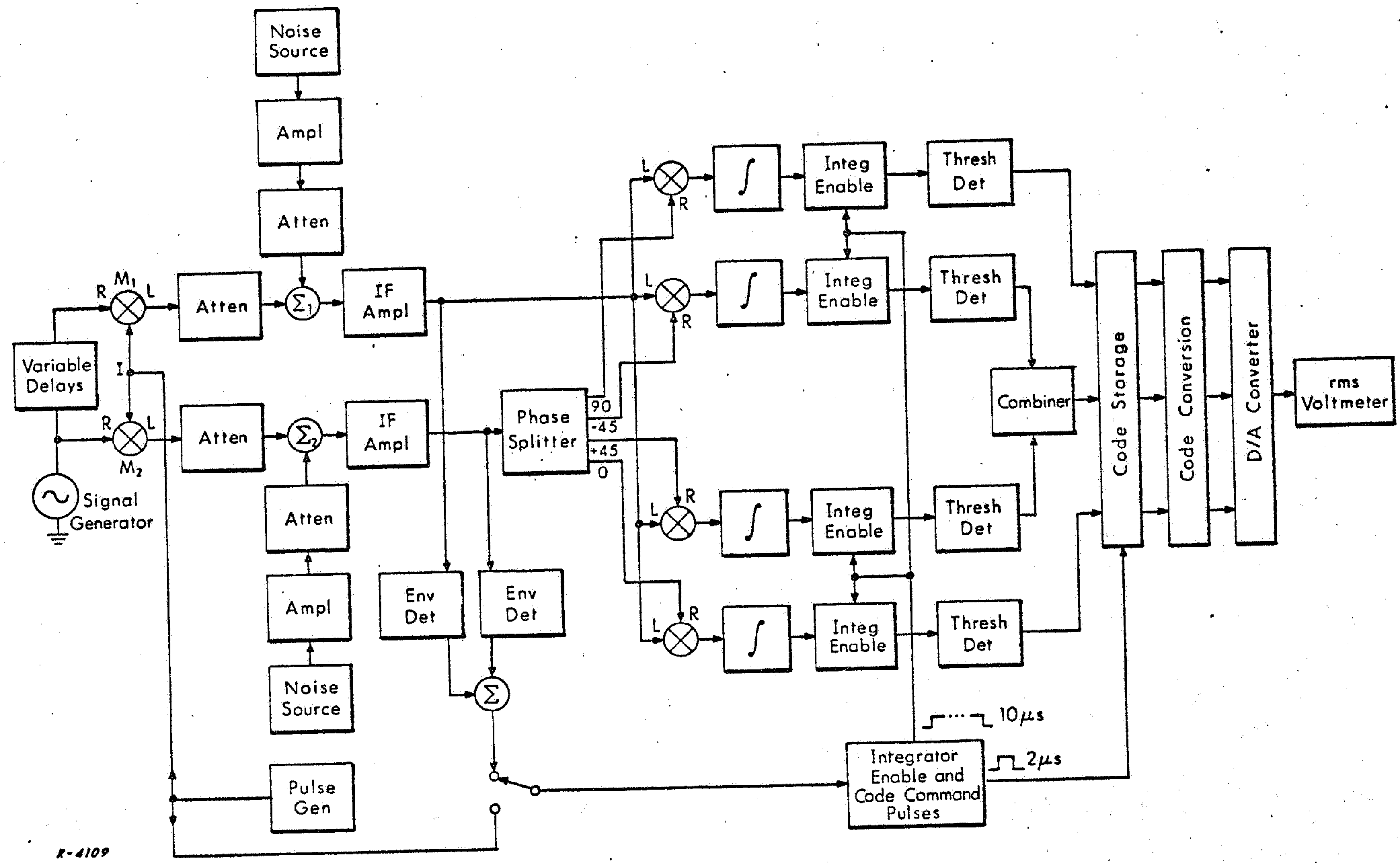


Fig. 4 Experimental Test Bed for Digital Phase Meter

and 360°. The coaxial lines were adjusted and calibrated using a sampling scope which displayed the phase shifted and un-phase shifted signals on a calibrated scope face. This gives the input phase difference to an accuracy of a few degrees which is adequate for the purposes of the experiment. This phase shifter is practically lossless so that the signals applied to the two balanced modulators M_1 and M_2 are of the same amplitude. The output of the pulse generator is also applied to M_1 and M_2.

Thus, the outputs of the two balanced modulators are 2 μsec pulses of equal amplitude occurring at a 50 kHz rate. The carrier phase of one of the pulse trains is controlled by varying the phase shifter setting. These modulators are followed by variable attenuators for control of input amplitudes. Noise is added to the input signals in the summers Σ_1 and Σ_2. Separate noise sources using diode noise generators followed by amplifiers and attenuators are used to ensure that the noises are independent as would be the case in real equipment using separate receivers for each antenna. The signal from each summer is passed through an IF amplifier for adjustment of levels and to provide realistic pulse response by virtue of filters incorporated in the amplifiers. Signals are tapped off the outputs of these amplifiers and applied to envelope detectors for initiation of system command and trigger pulses as described below. Alternatively these command and trigger pulses are initiated from the external pulse generator and the figure shows the alternative switching arrangement.

The two inputs, reference and signal, are then introduced into the digital phase detector. The reference signal passes through the phase splitter where it is split into four signals of relative phases 0°, $\pm 45^{\circ}$ and 90°. These signals are then applied as the reference signals to the four coherent detectors consisting of mixers and integrating networks. These integrators are rendered operative by an integrator enable network controlled by an integrator enable trigger pulse as shown in the figure. The integrator outputs drive the threshold detectors which employ integrated circuit comparators. The ambiguous output in the $\pm 45^{\circ}$ channels is resolved in the combiner by an "exclusive or" logic module.

The result of these operations is a 3 digit gray-coded word giving the phase measurement of the signal channel relative to the reference channel. This number is applied to the code storage circuits which consist of integrated circuit "D" type edge-triggering flip-flops. The code storage maintains the output at its last level until a change occurs. These units change state only if the input changes state while they are strobed at the repetition rate. Without this storage provision, the gray coded output would be strobed at the command repetition rate. With the present arrangement the output changes only if there is an input phase change or a noise induced measurement error.

The gray coded output of the code storage unit is then converted to a natural binary output in the code conversion unit. This conversion is obtained using integrated circuit digital logic modules.

In order to display the results of the phase measurement the following procedure is used. The natural binary coded output is converted to an analog voltage using a simple A/D converter employing weighting resistors. An rms voltmeter is calibrated using the phase meter without the noise sources connected. The volt meter is calibrated at each setting of the input phase shifters. The desired signal to noise ratio is then established by adjustment of the noise channel attenuators, and the rms phase error resulting from the addition of noise to the channels read directly from the meter.

3.2 System Timing Sequence

This section describes in detail the time sequence of events involved in making a digital phase measurement on a single pulse. Repetition rates as high as 5×10^4 pulses/second are allowed for in the design to account for random access by non-overlapping interrogators. Figure 5 illustrates the time sequence of triggering and command pulses.

A phase measurement on an individual incoming pulse is initiated in the following way. For simplicity the case is considered in which both the signal pulses and the measurement system trigger pulses are derived from the pulse generator. Consider the system at least 10 μsec after a measurement has been completed and while the arrival of the next input pulse is awaited. At this stage of the measurement procedure the integrator output is disabled or held to zero, the threshold detectors are at zero output and the code storage output is maintained at its last command setting.

Upon receiving the next command pulse (generated simultaneously with the next signal pulse in this configuration) the measurement sequence begins. Note that the command pulse is a 2 μsec pulse occurring at a 50 kHz rate for the purposes of this experiment. The choice of pulse widths is in no way critical and was made for convenience in completion of the breadboard. The circuitry could be modified to accommodate the full range of pulse widths normally used with standard instrumentation radars.

Referring to Fig.5, the leading edge of the 2 μsec command pulse (a), triggers a 10 μsec integrator enable pulse (b) which allows the integrators to begin operation after being held off. The integrators have a time constant set at approximately 5 μsec for this experiment. The outputs of the integrators drive the threshold detectors whose outputs will assume 1 or 0 states depending on whether positive or negative signals appeared at their inputs.

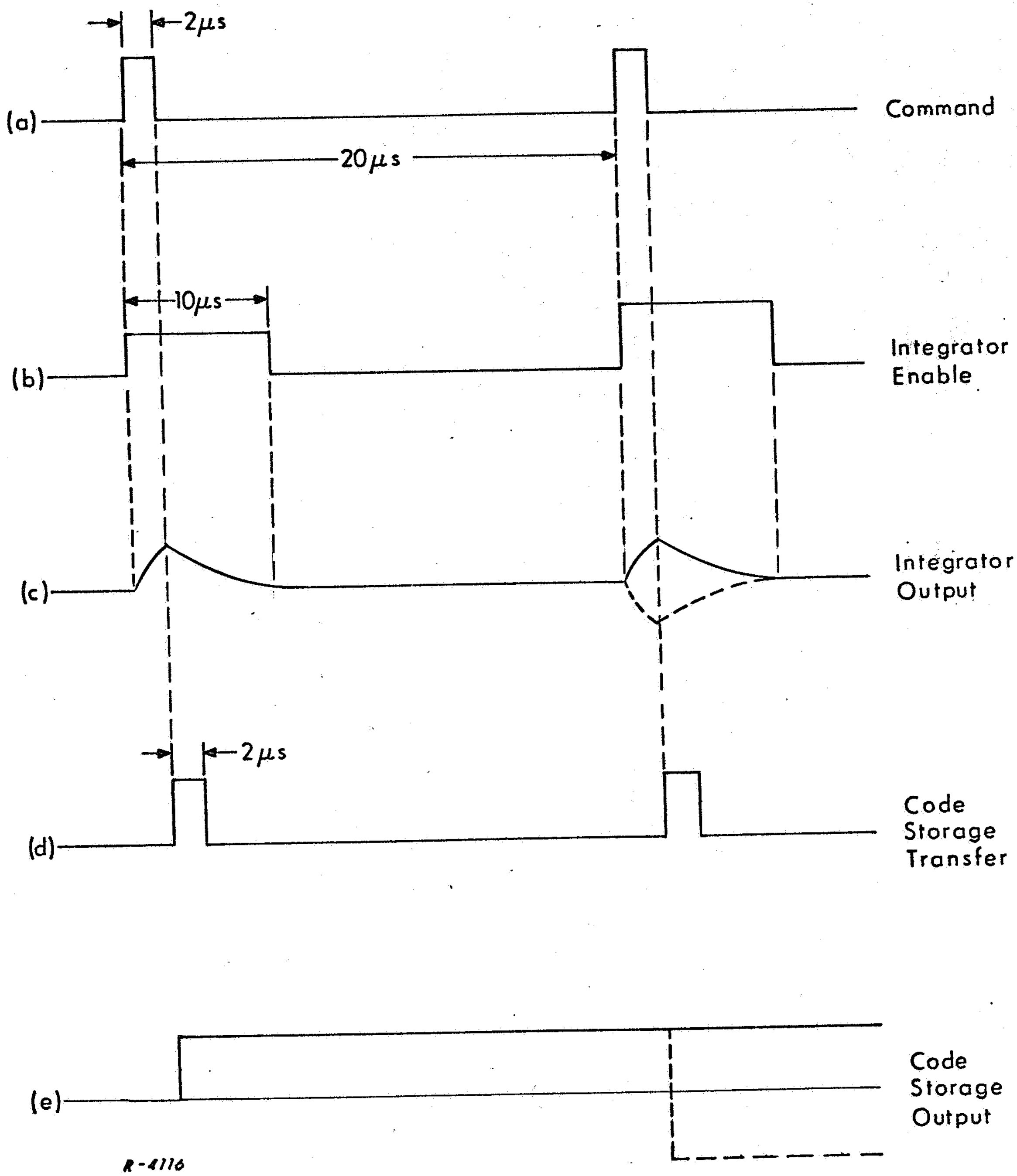


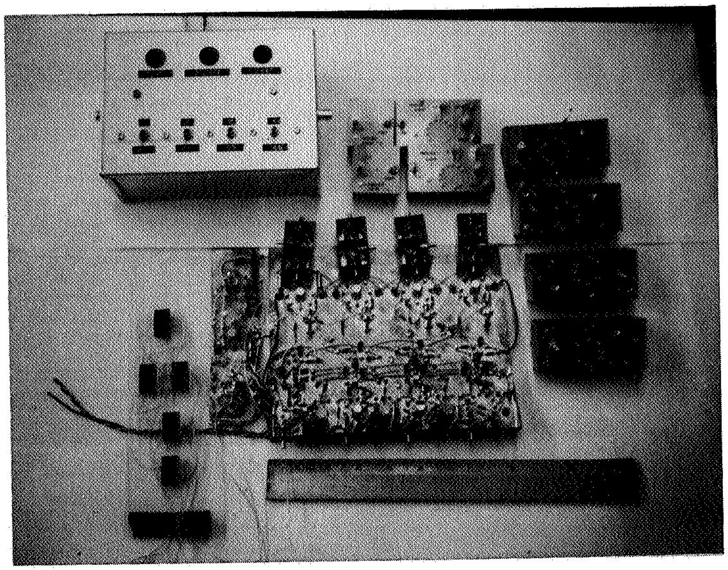
Fig.5 Measurement Timing Sequence

The trailing edge of the 2 μsec command pulse triggers a 2 μsec code storage transfer pulse shown in (d). This pulse transfers the output of the threshold detectors into the code storage circuits. The threshold detector output is sampled at the end of the 2 μsec command pulse since the integrator output is maximum at this time and starts decaying afterwards. The code storage unit maintains its state until two conditions are satisfied simultaneously, namely, the arrival of another command pulse and a change of state of the threshold detector output. The code storage output is shown in (e).

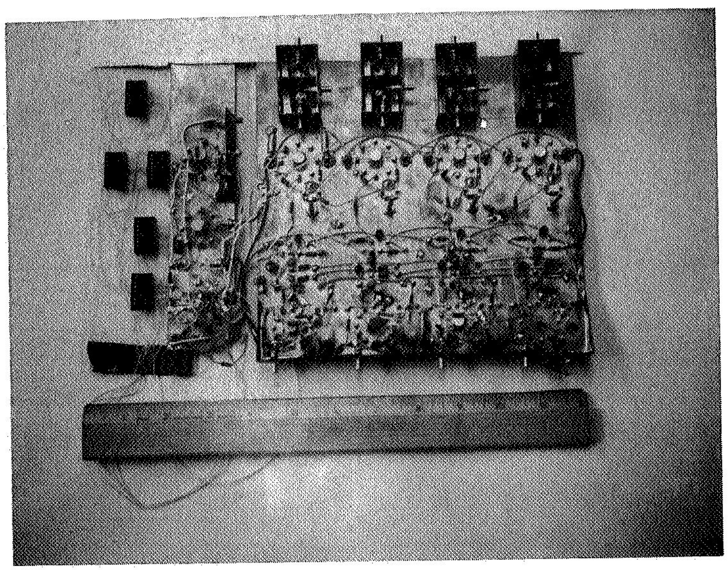
The final operation in the sequence is initiated by the trailing edge of the 10 μsec integrator enable pulse. This automatically disables the integrator circuit and holds it at ground, thus restoring the system to its quiescent interpulse condition.

The discussion of the timing sequence given above for simplicity assumes that the system command pulse is derived from the pulse generator forming part of the experimental test bed. During the experimental work the system command pulse was also derived by envelope detecting the outputs of the reference and signal IF channels before these were applied to the phase meter itself. This simulates operational use of the phase meter. In that case, the system command pulse must be triggered by the actual arriving signals. In operational use, the trigger is derived by averaging the envelope detected outputs of all the IF amplifiers and using the resultant video pulse to drive a threshold detector.

Photographs of the actual breadboard circuitry used in carrying out the experiment are shown in Fig. 6. Figure 6 (a) shows the phasemeter and associated IF amplifiers, noise sources, output phase shift display, code storage and converter, and switched phase shifters. Figure 6 (b) shows only the digital phase meter and code storage and conversion modules. The possibility of considerable reduction in package size is apparent from the latter photograph.



(a)



(b)

Fig. 6 Digital Phasemeter Experimental Breadboards

4. EXPERIMENTAL RESULTS

The experimental results showing rms phase error vs input signal to noise ratio for each setting of the variable phase shifter are shown in Figures 7 through 12. Figures 7 through 9 show the results using an external trigger derived from the pulse generator to clock the system, while Figures 10 through12 show the results obtained for a self-generated trigger.

The performance of the system for SNR's greater than 13 dB is adequate in all cases, and in most cases rms phase errors no greater than 45° are obtained for SNR's of 4 dB. It is important to note that in some of the cases the quantization error, $22\text{-}1/2^\circ$, must dominate for intermediate SNR's. In one case, namely for an input phase setting of 295°, it is suspected that one of the phase detectors was operating with zero phase difference at its inputs. Thus the time phase is exactly half way between two possible digital phase settings, and the digital output, in the absence of noise, should jump between the two adjacent readings. This is a possible explanation for the anomalous error readouts for this input phase setting for either triggering mode.

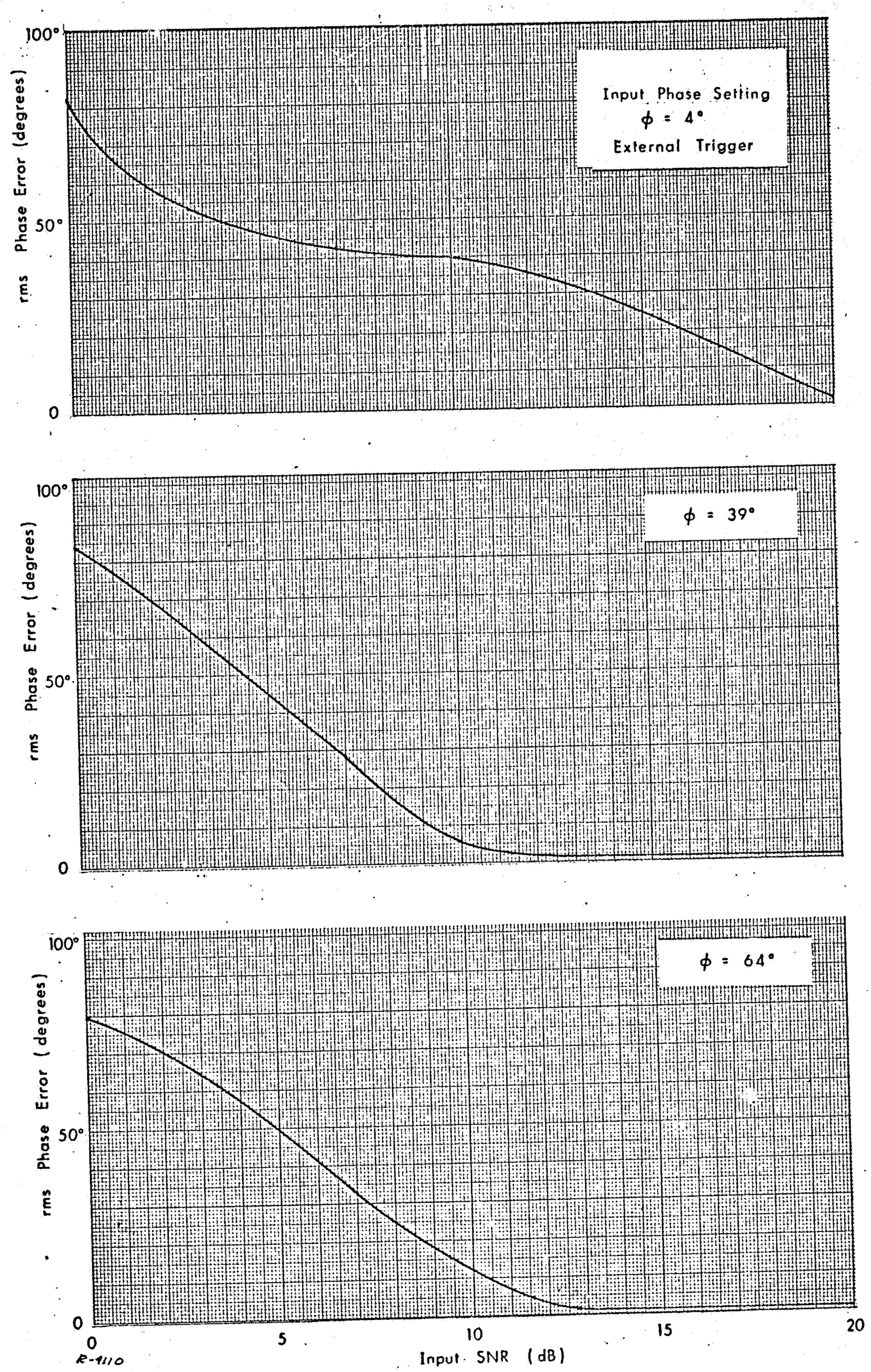


Fig. 7 rms Output Phase Error vs Input SNR

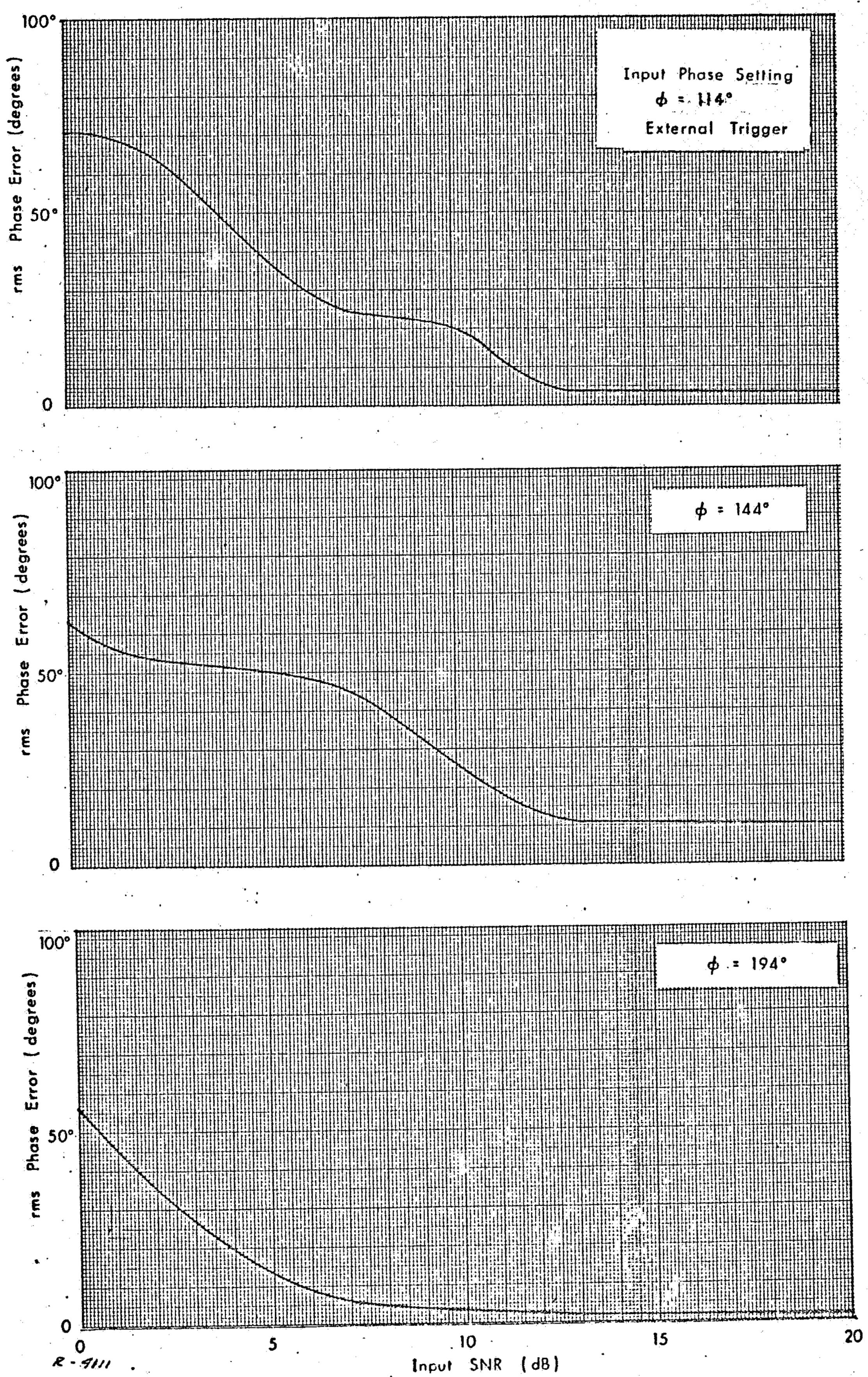


Fig. 8 rms Output Phase Error vs Input SNR

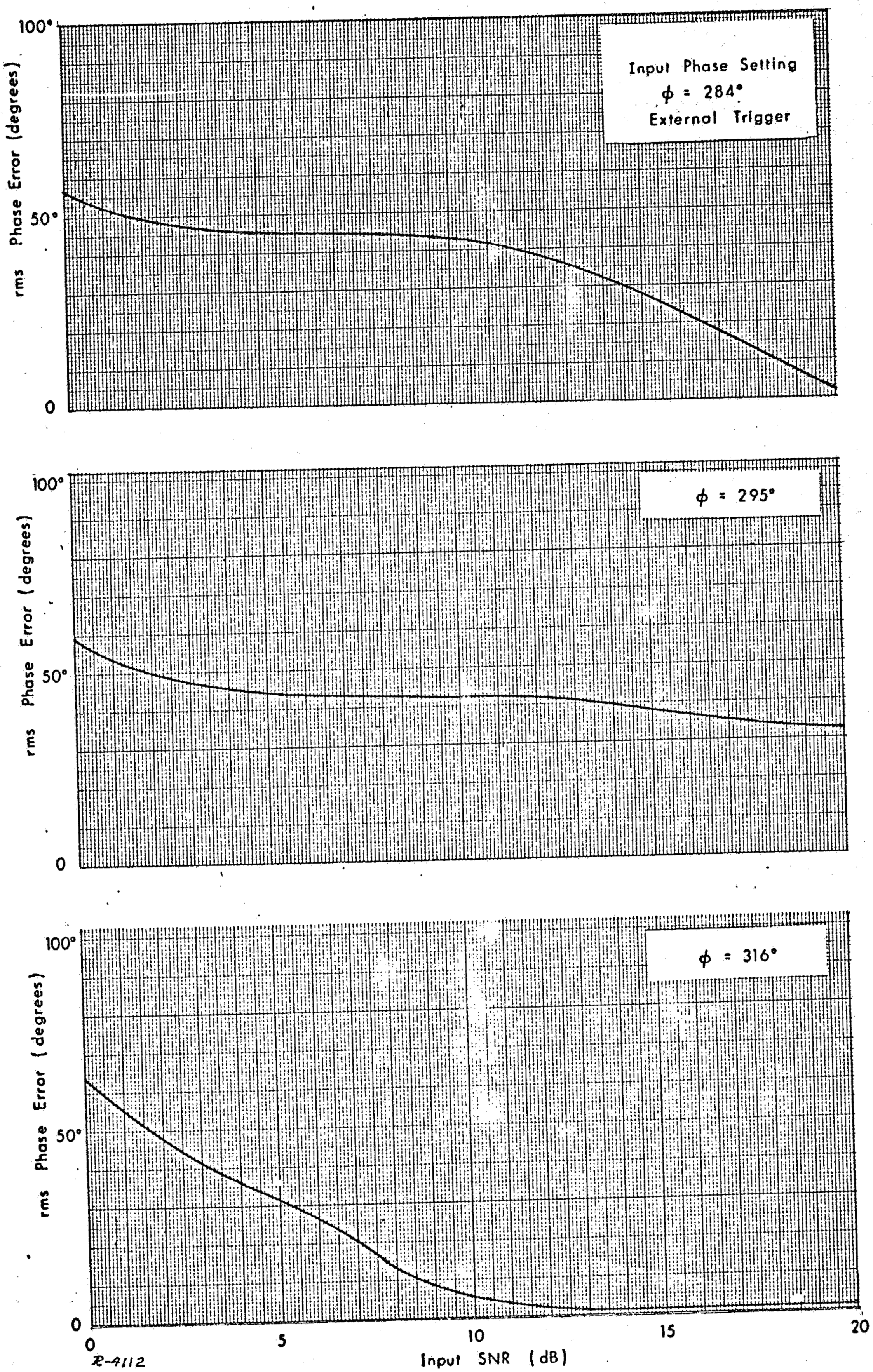


Fig. 9 rms Output Phase Error vs Input SNR

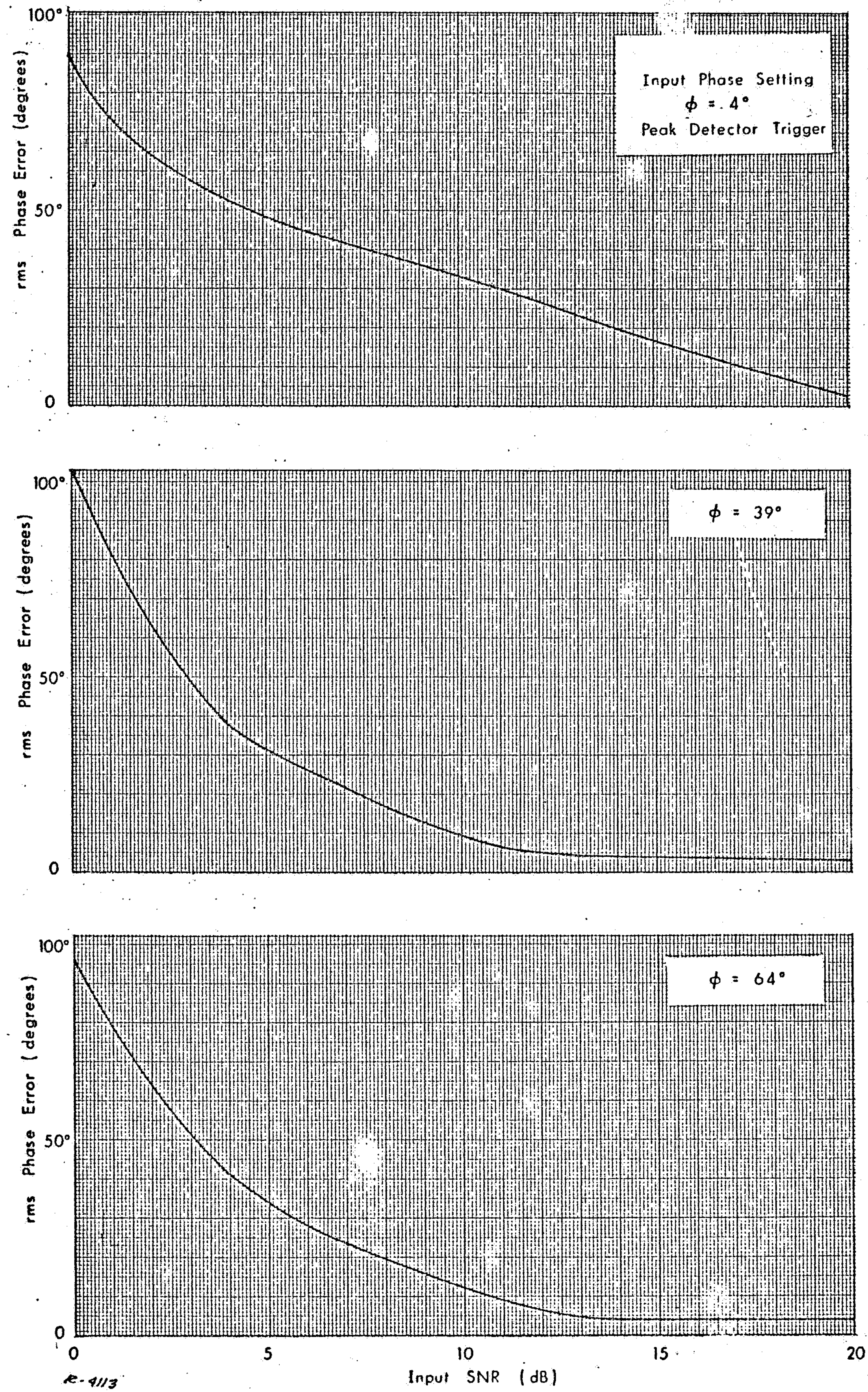


Fig. 10 rms Output Phase Error vs Input SNR

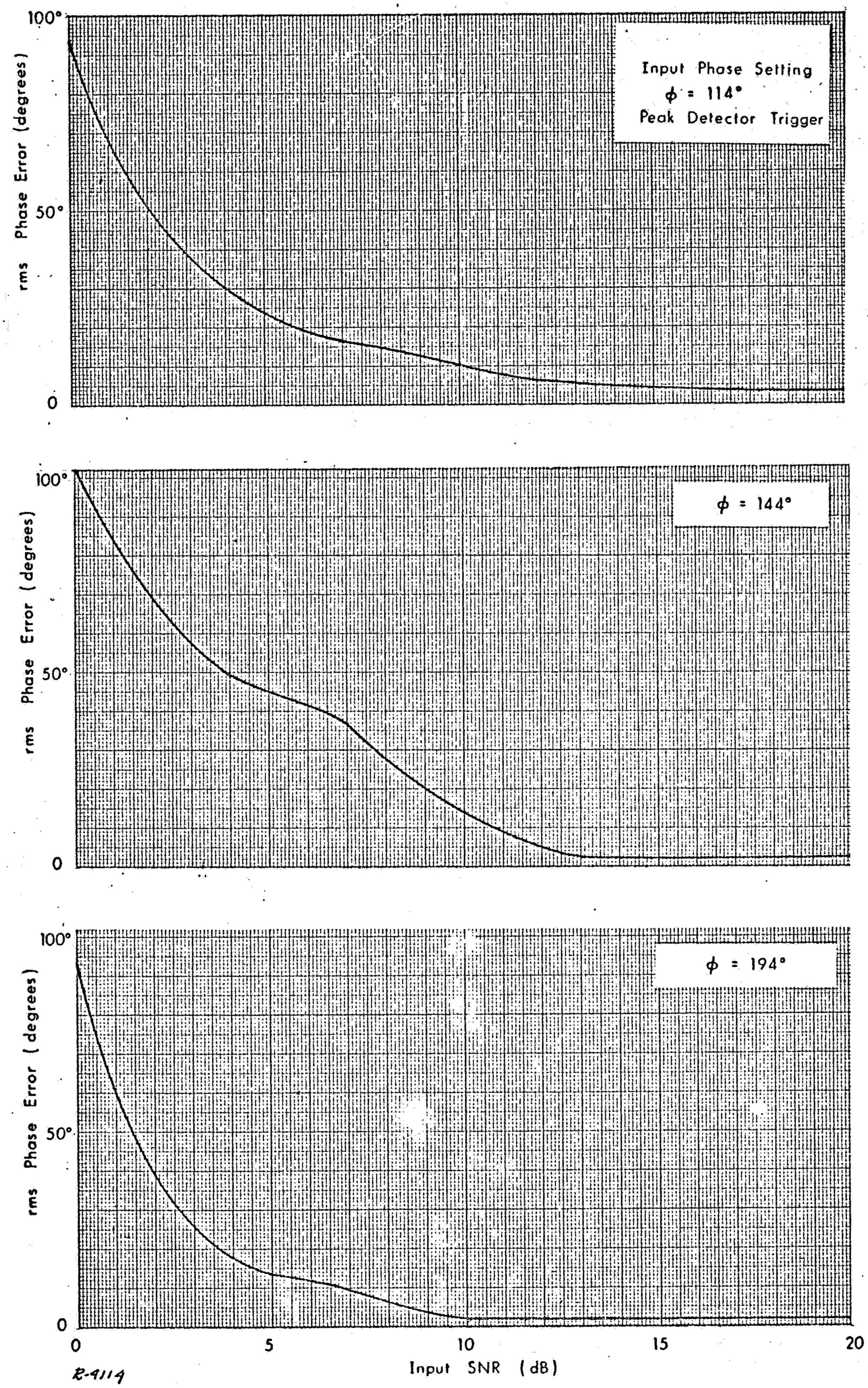


Fig. 11 rms Output Phase Error vs Input SNR

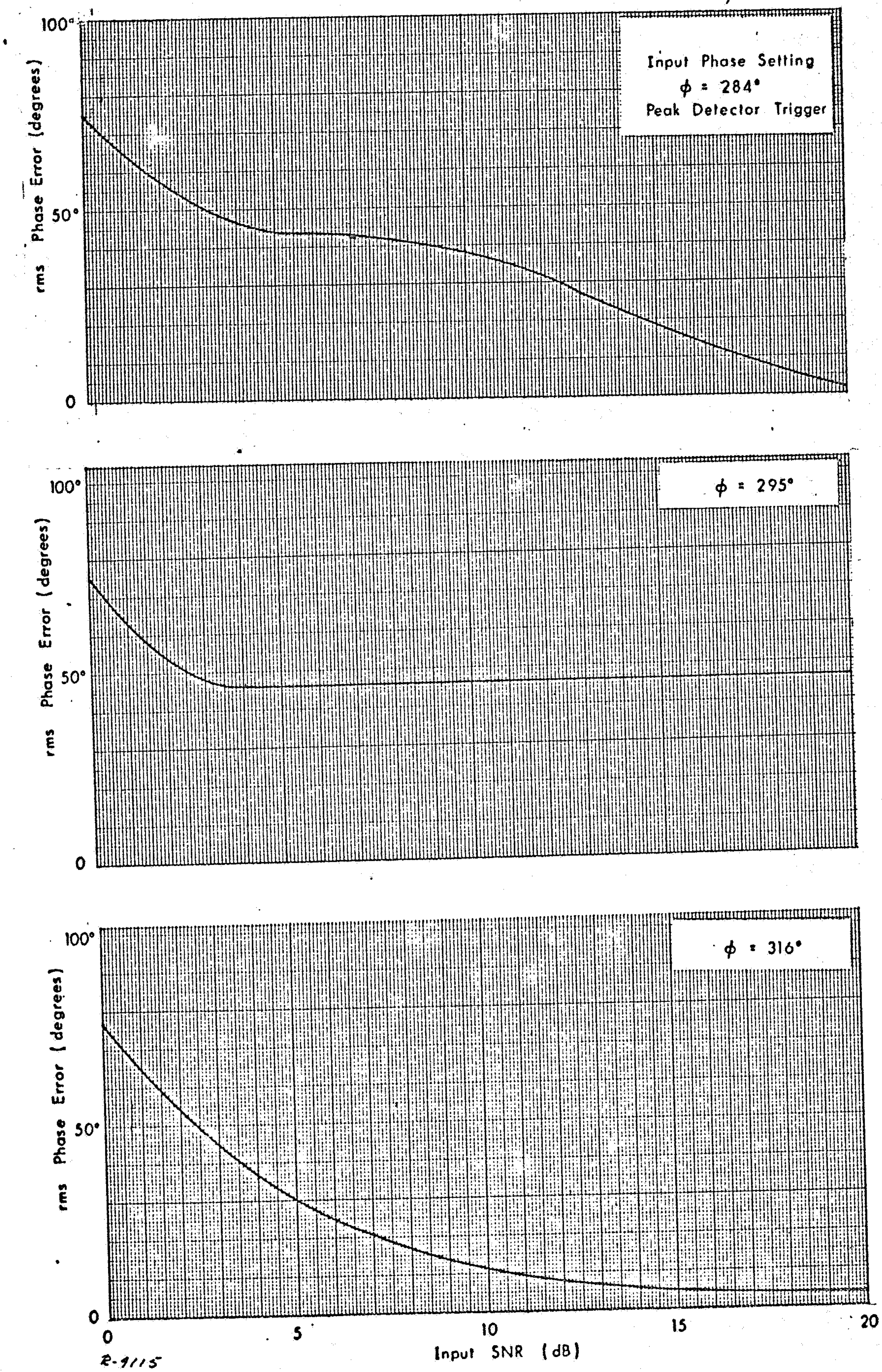


Fig. 12 rms Output Phase Error vs. Input SNR

5. CONCLUSIONS AND RECOMMENDATIONS

A breadboard version of the digital phase measuring subsystem of the pulse-coherent retrodirective transponder has been successfully constructed and tested. The phase measurement subsystem makes use of an octonary detector typically employed in digital PSK systems. No unusual problems were encountered in the design and implementation of a breadboard digital phase meter and in carrying out a test program designed to yield realistic performance data.

Earlier work carried out in a related study[2] showed that an uplink SNR of 4 dB gave an rms phase error at the output of a phase detector above threshold of approximately 45°. The present experimental work has confirmed these earlier conclusions. For many cases measured rms phase errors were below 45° for an input SNR of 4 dB and this was maintained for both internal and external system triggers. With one exception the rms output phase error falls rapidly with improved input SNR. The anomalous case corresponds to an unstable phase detector condition which yields the maximum noise due to quantization effects. However, even in this case the rms phase error of the output or retransmitted signal corresponds to a maximum array gain reduction of only 3 dB. Thus the present retrodirective technique appears well suited for this specialized application involving unfocussed (no pilot tone) uplink detection and high-powered, non-overlapping multiple interrogation.

It is recommended that the present basic experiment be extended to include a fuller realization of the overall system. This would include breadboarding of the microwave portions of the input circuitry, detailed experimental verification of system detection characteristics, integration of digital phase shift elements into the design, and study of optimum TWT keying circuitry. It is felt that the basic technique offers a practical and successful alternative to previous Saturn antenna configurations and that further study should be given to the precise trade-offs possible between increased complexity and weight and power reductions. It is also recommended that further study be given to possible application of this technique to the general problem of multiple access satellite communication systems.

REFERENCES

1. "Retrodirective Arrays for Pulse-Coherent Transponders," H.Salwen, ADCOM Technical Memorandum, Reference NAS8-20001, 12 July 1966.

2. "Application Notes for Pulse-Coherent Retrodirective Arrays," H. Salwen, ADCOM Technical Memorandum, Reference NAS8-20001, 6 October 1966.

3. "Data Transmission," Bennett, W.R. and Davey, J.R., McGraw-Hill Book Company, 1965.